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A LOW POWER LDO REGULATOR WITH SMALLOUTPUT VOLTAGEVARIATIONSAND HIGH PSRR IN 0.18µm CMOS TECHNOLOGY

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ABSTRACT: A low dropout voltage regulator with small output voltage variations and the ability of wide load current range support is proposed in this paper. In this LDO structure, a recycling folded cascode operational transconductance amplifier is used as an error amplifier, which has high transconductance and therefore high power efficiency. The designed LDO is simulated in 0.18 µm CMOS standard technology and has small output voltage variations about 48 mV for load current in the range of 0-150 mA. Simulation results show a favorable transient response behavior with 4.2 µs rise time and 160mV dropout voltage for current changing in the desirable range. It is shown that the LDO structure can support 0-150 mA load current range with reasonable output voltage variations. In addition, with the smaller load current ranges, the dropout voltage will be higher and the output voltage variations will be smaller.

Keywords: low noise; transient response; power consumption; buffer; load current changes.

INTRODUCTION

The recent trend toward the on-chip circuit design has led to using several analog blocks on a chip surface, so these circuits suffer from noise on power supply lines. Noise can effectively degrade the entire system performance by reducing the dynamic range. LDO voltage regulator has low noise, simple circuit structure and high ripple rejection characteristics which all make it a vital building block in portable electronic devices. Despite input voltage variations and load current changes, a LDO voltage regulator is designed to create a stable voltage, however, considering the range specified by manufacturers. Low dropout voltage makes the LDO voltage regulator appropriate for wireless and portable applications, so dropout voltage for this circuit is one of the most important characteristics. On the other hand it has to be noted that noise can significantly reduce the performance of the accurate and sensitive circuits. So another most important characteristic is low noise performance. There are some techniques to decrease noise of the operational amplifiers that are usually used as an error amplifier part in LDO regulator design. According Sobhy et al. (2010), two methods to decrease noise at both DC and higher frequency are used. The first method uses a high pass filter whereas the second one is based on the cross coupled design that consists of matched resistors and capacitors which causes PSRR improvement. However using this structure in the LDO regulator design causes a decrease in noise but degrades the gain bandwidth and slew rate and therefor transient response in the LDO regulator. There is a tradeoff between transient response behavior and power consumption in the LDO regulators. In addition, low dropout voltage and high load current delivery should be considered. Although it is not possible to achieve all desired characteristics simultaneously, one can be totally optimized. There are several techniques to achieve fast transient response for LDO regulators, such as capacitive coupling from output of LDO to the biasing circuits (Or and Leung, 2010; Guo and Leung, 2010). Also an additional

amplifier was inserted into the feedback path to improve steady state performance (Guo and Leung, 2010). Insertion of the additional amplifier degrades the stability and occupies more area. An on-chip FVF-based LDO design is demonstrated in (Lai and Li, 2012), which used multiple feedback loops. Although in this design a frequency compensation plan has been suggested to improve the LDO stability, but the quiescent current and power consumption are high. Using a well-designed feedback network and a current feedback buffer amplifier (CFB) seems to be a suitable solution, however this technique has only improved transient response but power consumption is not desirable (Wang et al., 2010). Several methods are presented to reduce the power consumption of the LDO regulator structure. One of these methods is to use a low-voltage buffer and a circuit to improve the slew rate (Shen et al., 2008). The mentioned method provides a large dynamic current to charge and discharge capacitor at the gate of pass transistor at the output stage of the LDO regulator. In some cases, with current mode buffer, the LDO achieves fast response with small output capacitance, but in these cases, the quiescent current and therefore power dissipation is high (Oh and Bakkaloglu, 2007). According to Miliken et al. (2007), LDO regulator has used a compensation circuitry to improve stability and reach a desirable transient response. The advantage of this circuit is small output voltage variations but in the contrary it suffers long settling time and high quiescent current.

Here to increase the gain-bandwidth product and thus the power efficiency an operational transconductance amplifier (OTA) is used as an error amplifier. Also, to improve the transient response, a feedback circuit at the output stage and a buffer circuit in the middle stage have been used.In section 2, the proposed LDO regulator circuit will be described in detail. The simulation results of the proposed LDO regulator will be explained in section 3. Finally, in section 4, the conclusion will be provided briefly.

IMPLEMENTATION OF THE PROPOSED LDO REGULATOR CIRCUIT

As shown in the figure 1, the proposed LDO regulator components include an error amplifier for the first stage, a compensation circuit for the middle stage and a power transistor with a feedback network for the output stage. Usually a buffer circuit is used as compensation circuit to guarantee a good stability for general LDO design.

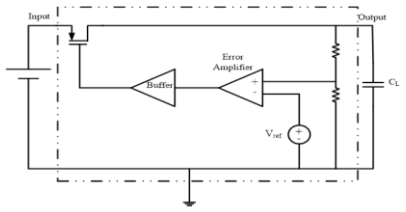

Figure 1. LDO Block Diagram

In this LDO structure, the OTA is used as an error amplifier (EA) which provides desirable transconductance and therefore voltage gain for the circuit. Since this OTA design provides separated pathway for AC and DC currents, therefore the PSRR for LDO regulator can be improved. The OTA circuit also has a good slew rate, thus the transient response of the overall LDO circuit is desirable. As shown in figure 2, the OTA circuit has a folded cascode scheme with separated DC and AC path. In the proposed OTA circuit, the DC currents can pass through M_5, M_6, M_7 and M_8, M_9, M_{10}. Since M_7, M_{12} and M_8, M_{13} have high impedance for AC currents so that almost no AC current will pass through these paths. As a result, different pathways can be considered. Consequently it can be said that AC current mirrors are M_5, M_6 and M_9, M_{10} and DC pathway can be considered in M_7, M8 transistors. This method of separating AC and DC pathways, can lead to an increased transconductance.

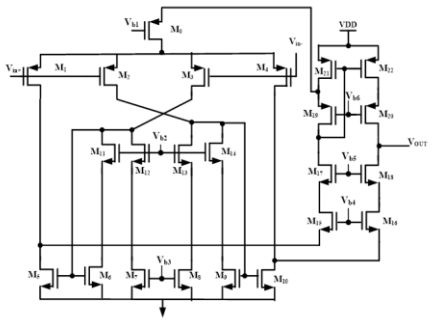

Figure 2. Proposed OTA as an error amplifier

To achieve better results, transistor ratios can be considered as the following:
Assuming γ as M_1, M_4 transistors ratio, for input transistors, it can be written:

$$\frac{(W/L)_1}{(W/L)_2}=\frac{(W/L)_4}{(W/L)_3}=\frac{\gamma}{1-\gamma} \quad (1)$$

Which, W and L are introduced as width and length of transistor channel respectively.
The M_5, M_6, M_7 and M_8, M_9, M_{10} ratios can be considered as:

$$\frac{(W/L)_5}{(W/L)_6}=\frac{(W/L)_{10}}{(W/L)_9}=\frac{1+\gamma}{p(1-\gamma)} \quad (2)$$

$$\frac{(W/L)_6}{(W/L)_7}=\frac{(W/L)_9}{(W/L)_8}=\frac{p(1-\gamma)}{q(1-\gamma)} \quad (3)$$

While, $p + q$=1, assuming p and q as constant values.
For M_{11}, M_{12} and M_{13}, $M_{14;}$ it can be considered the following:

$$\frac{(W/L)_{11}}{(W/L)_{12}}=\frac{(W/L)_{14}}{(W/L)_{13}}=\frac{p}{q} \quad (4)$$

It can be expressed that M_6, M_9 are driven by input pairs while M_7, M_8 are biased by a constant voltage that is applied at the gate.

By choosing $\gamma=p=1/2$ a desirable transconductance is expected for the EA. On the other hand, the output resistance of M_1, M_4, M_5 and M_{10} is high so the gain bandwidth product is increased. Increasing the gain bandwidth product for EA part causes the output voltage variations of LDO to decrease. Using this structure for EA part, the slew rate for LDO can also be improved.

It should be noted that to achieve a low power behavior in the LDO design, one path between the source terminal of the M_0 and drain terminal of M_{21} is used as shown in the figure 2.

The proposed LDO structure is shown in figure 3. The buffer circuit guarantees the LDO design stability with adding zero-pole pairs and by removing non-dominant poles.

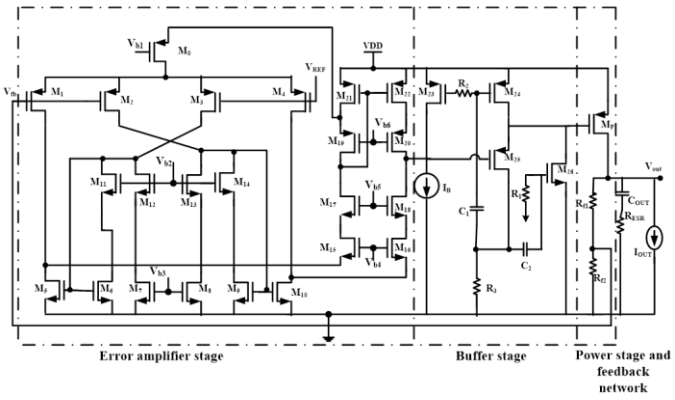

Figure 3. Proposed LDO structure

By applying an appropriate voltage to the V_{REF} and a feedback path from the output to another input of the LDO circuit, and biasing some transistors in triode and subthreshold, power consumption is reduced, while speed of the total LDO circuit increases.

Since the output of the error amplifier is applied to the next stage transistor gate, therefor a significant output resistance is needed. The following equation can be obtained for EA output resistance:

$$R_{O(EA)} \approx r_{o18}\{1+g_{m18}r_{o16}[1+g_{m16}(r_{o4}\| r_{o10})]\}\| r_{o20}[1+g_{m20}r_{o22}] \quad (5)$$

Which $R_{O\,(EA)}$ is EA output resistance, g_{m16}, g_{m18}, g_{m20} are M_{16}, M_{18}, M_{20} transconductances and $r_{o4}, r_{o10}, r_{o16}, r_{o18}, r_{o20}, r_{o22}$ are output resistances of M_4,M_{10},M_{16},M_{18},M_{20},M_{22} respectively.

Thus, by connecting the second stage, it is expected that the problem of second stage loading on the EA output stage will not happen for general LDO circuit.

The main poles and zeros of the LDO circuit are respectively as following:
The loading of the pass device or power transistor on the EA will create first pole.

$$P_1 = \frac{1}{2\pi R_{O(EA)} C_{gate(MP)}} \quad (6)$$

Which $C_{gate\ (MP)}$ is gate capacitance of the power transistor.
Output capacitance (C_{OUT}) will add another pole as well.

$$P_2 = \frac{1}{2\pi R_{Load} C_{OUT}} \quad (7)$$

While, R_{Load} is load resistance of the proposed LDO circuit.
Electrical series resistance right hand plane (ESR RHP) zero may be the most low frequency zero.

$$Z_1 = \frac{1}{2\pi C_{OUT} R_{ESR}} \quad (8)$$

There are several non-dominant poles and zeros too, but the buffer part and also C_C help the LDO stability by removing these poles and zeros and most important of them are mentioned above.

SIMULATION RESULTS

The proposed LDO regulator is implemented in 0.18 µm standard CMOS technology. It has a reasonable bandwidth, good stability and phase margin at 0-150 mA load current variation as shown at the magnitude and phase of loop gain in figure 4. By applying a 1.8 V supply voltage, the dropout voltage is about 160 mV for 0-150 mA load current range. Simulation results show good transient response as shown in figure 5. For 0-100 mA load current changes the dropout voltage is about 173 mV and the output voltage variation is about 24mV. For 0-50 mA load current changes the dropout voltage is about 183 mV and output voltage variation is about 9 mV with small rise time about 1.2 µs. Although 0-50 mA load current range has very small output voltage variation but the dropout voltage is higher than the other two.

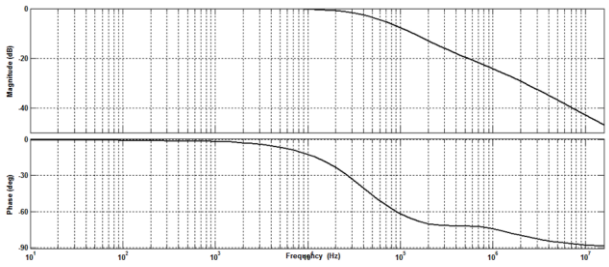

Figure 4.Magnitude and phase of loop-gain

The proposed LDO regulator shows good response for 0-150mA load current changes. It shows very small and desirable output voltage variations about 48 mv that make the proposed LDO suitable for battery power applications. The quiescent current is low about 0.33 µA with power consumption about 0.6µW, so the proposed LDO regulator can be used for low power applications. The LDO circuit has a low noise structure and the simulation results for noise at several frequencies are shown in table 1.

According to the table 1, in comparison with the recently published LDOs, for 0-150 mA load current changes, the rise time is reasonable and small about 4.2µs. Also the ratio of $\Delta V_O/V_O$ is low, which leads to a very stable output voltage for the proposed LDO regulator. As shown in table 1, simulation results show that the output noise for 100 kHz, is very low and in the Pico volt range.

CONCULSION

It is very difficult to achieve low power and desirable transient response behavior for LDO circuits simultaneously, so an optimal choice should be considered. In the proposed LDO structure, favorable results for power consumption and transient response are achieved. In additional to the mentioned problem, LDO circuit stabilization is also an important issue. In this paper a buffer circuit provides a good result for compensation and stabilization of the proposed LDO. Also, a low dropout voltage and small output voltage variations are achieved under low power consumption. Therefore, it is expected that the proposed LDO regulator can be used in the power management section of the battery powered applications like cell-phones, pagers and so on.

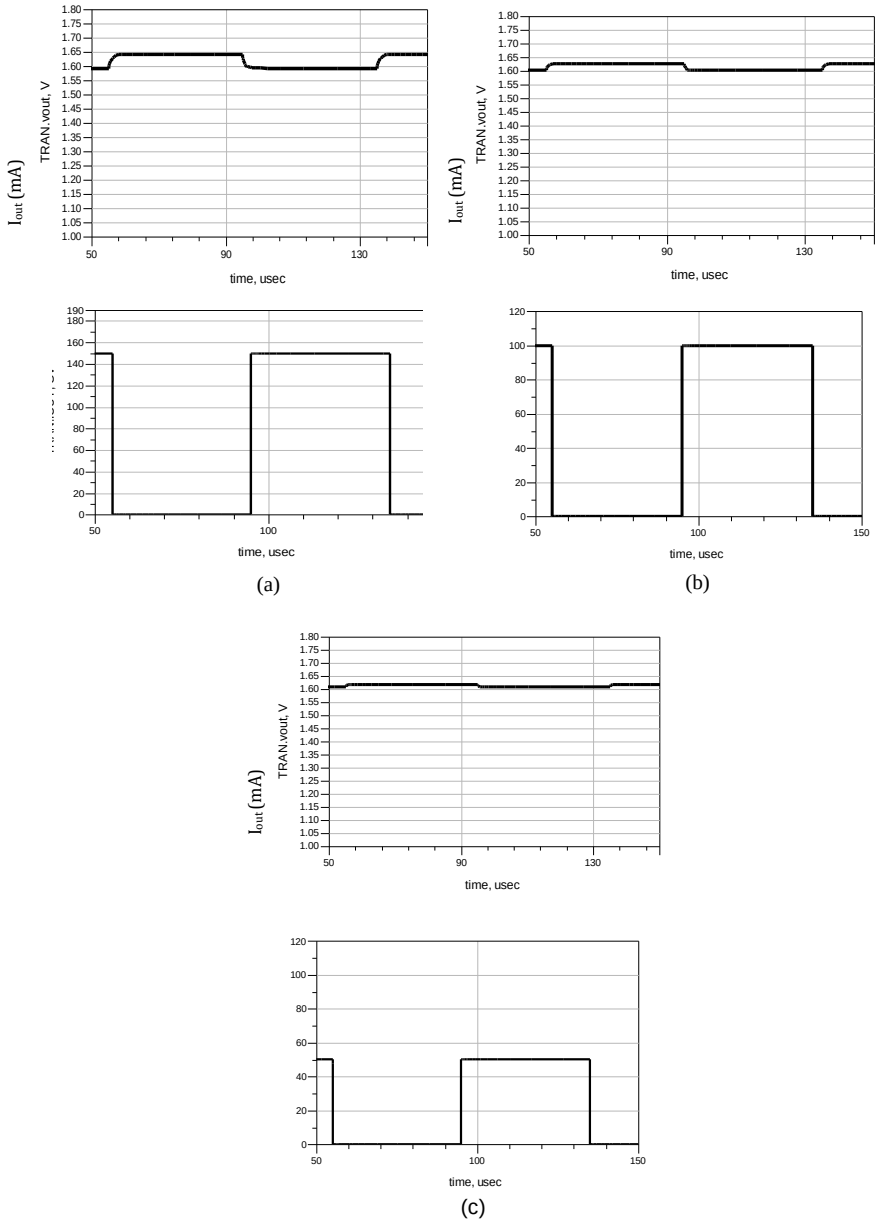

Figure 5. Transient response of the proposed LDO regulator (a)for 0-150 mA load current changes (b)for 0-100 mA load current changes (c)for 0-50 mA load current changes

Table 1. Performance comparison with previous proposed LDOs

Ref.	[2]	[4]	[5]	[6]	[7]	[8]	[9]	This work
Technology(μm)	0.35	0.25	0.35	0.35	0.35	0.18	0.5	0.18
V_{IN}(V)	1.2	2~2.5	3	2~3	1.8-4.5	1 – 1.8	1.4 - 4.2	1.8
Drop-out Voltage(mV)	200	300	200	200	200	100	200	160
V_O(V)	1	1.5~1.9	2.8	0.6~3.15	1.6	0.9	1.2	1.64
ΔV_O(mV)	75	-	90	60	-	700	120	48
$\Delta V_O/V_O$	7.5%	-	3.2%	~10%	-	77.8%	9.9%	2.92%
I_O(MAX)(mA)	5	50	50	200	100	50	100	150
I_q @I_O=0	0.06 mA	0.1 mA	0.065 mA	60 μA	> 20 μA	1.2 μA	45 μA	0.33 μA
T_r (μS)	0.94	-	15	8	9	-	-	4.2
Output Noise@100kHz	-	67.7 nV	0.63 μV	-	-	-	-	31.43 pV

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